

MADELEINE R. SPARKS

GRAPHICAL SYSTEMS SCIENTIST



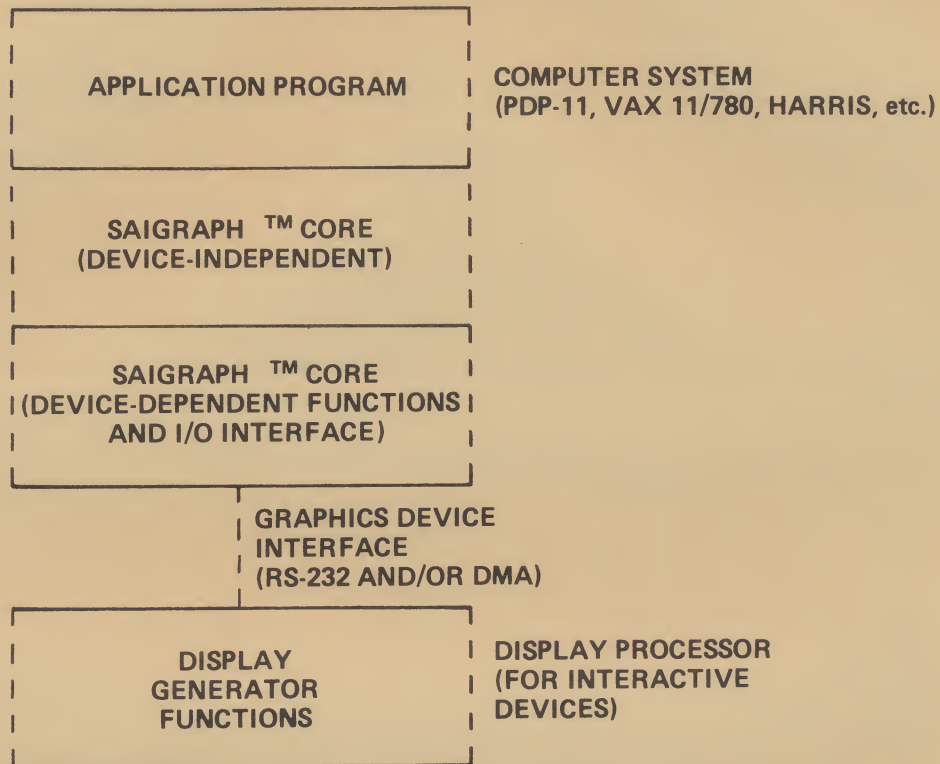
Science Applications, Inc.

2109 W. Clinton Avenue, Suite 800, Huntsville, Ala. 35805

Bus. (205) 533-5900



SAIGRAPHTM INTERACTIVE GRAPHICS CORE SYSTEM



THE SAIGRAPHTM Core Software System is a computer and device-dependent interactive graphics software package that is compatible with the ACM/SIGGRAPH proposed graphics standards.

SAIGRAPHTM is a graphic software engineering tool which can be called from FORTRAN user-level programs to create displays on and receive input from graphic devices. SAIGRAPHTM is implemented in FORTRAN and is available on the Digital Equipment Corporation PDP-11, VAX 11/780, and Harris computer families. Currently, support is available at the intelligent/non-intelligent level for raster, refresh, storage tube, and plotter devices (e.g., MEGATEK 7000, TEKTRONIX 4014, VERSATEC 1200/V80, CALCOMP 105X and RAMTEK RM-9400).



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Science Applications, Inc.
5 Wrigley Street
Irvine, CA 92714
(714) 951-1544

SYSTEM DESIGN

SAIGRAPH™ is divided modularly into device-independent and device-dependent portions. This design provides:

- The separation of input and output functions
- The minimization of the difference between producing output on a plotter and on an interactive graphics display
- The concept of two coordinate systems; the world coordinate system in which the picture for display is constructed, and the device coordinate system in which data to be displayed is represented
- The concept of a display file, containing device coordinate information
- The notion of display file segments, mutually independent, each of which can be independently modified as a unit
- The provision to transform world coordinate data into device coordinates by invoking a viewing operation

SAIGRAPH™ is further divided into input and output functions. Input routines support both synchronous and asynchronous (queued) input for keyboard, joystick, function button, pick and locator (graphic cursor) devices. Output routines accept generic graphic functional parameters from the application program for translation to specific graphic devices. SAIGRAPH™ output routines provide:

- World coordinate to display device position transformations
- Pixel and vector processing
- Image transformation
- Retained and temporary segments
- Dynamic segment and static primitive attributes
- Batching of display updates
- Clipping
- Image mode processing
- Error notification
- Line drawing for a single vector or series of connected vectors
- Current drawing position maintenance
- Drawing single or series of marker symbols
- Absolute or relative mode coordinate notation
- Geometric symbol macros
- Text processing
- Conic functions
- Windows and viewports

Control in SAIGRAPH™ is divided into three separate areas: Core, View Surface and Segment Control. Core control initializes and terminates the SAIGRAPH™ system and the display devices which will be used. View surface control maintains the display integrity (e.g., when a display becomes invisible or updated). Segment control creates, deletes, copies, and manipulates dynamic attributes (e.g., visibility, highlighting, detectability).

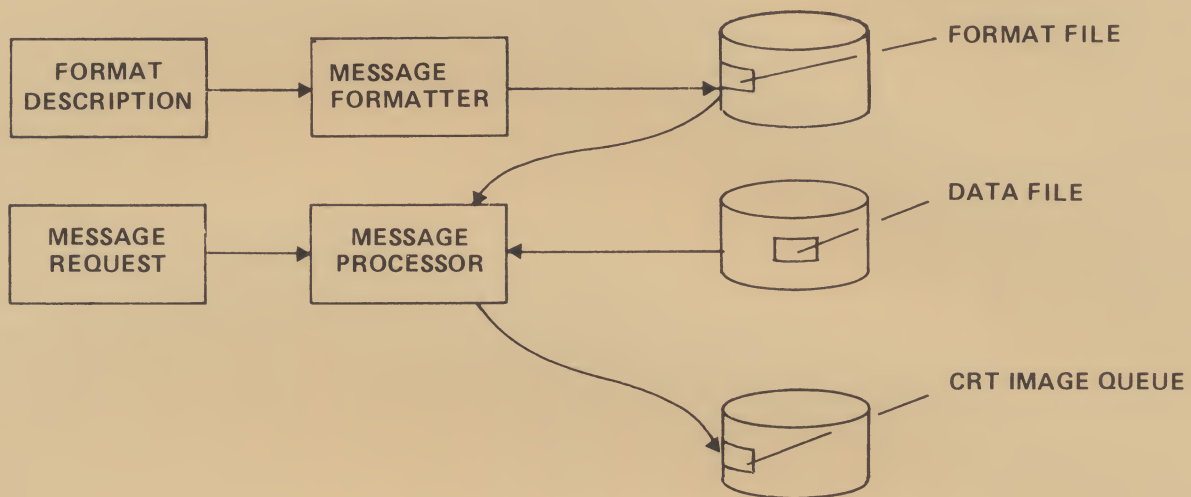
Full SAIGRAPH™ support, including installation, training, correction/update, enhancement, HOT-LINE and consulting services, is available from the SAI Computer Productions Division.



MSGFMT/MSGPRO

MESSAGE FORMATTER AND MESSAGE PROCESSOR

FOR THE CREATION OF A USER-DEFINED CRT IMAGE



MSGFMT provides a facility to create an ASCII CRT image skeleton from user-defined input. This image skeleton is saved in a disc file and is used by MSGPRO to merge user-supplied data with the image skeleton and create a CRT image. The image is placed in a disc queue for display at the user's command.

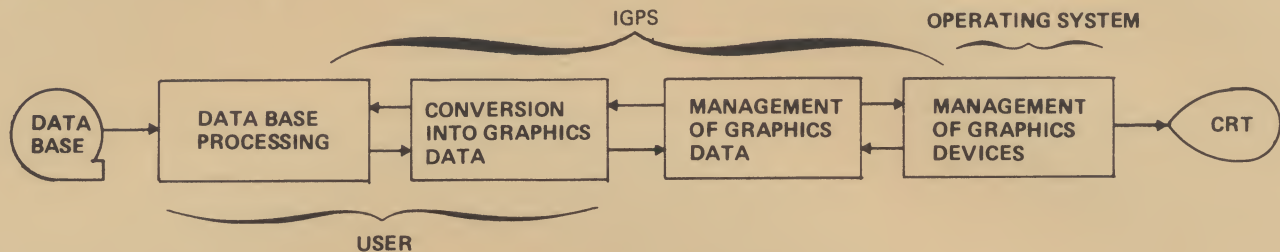
MSGFMT and MSGPRO are coded in FORTRAN IV and are currently operational on a PDP-11 with a Perkin-Elmer OWL CRT terminal. The CRT image queue processor is a user-supplied task.



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IGPS INTERACTIVE GRAPHICS PROGRAMMING SYSTEM



The Interactive Graphics Programming System (IGPS) is a three-dimensional software package which resides in the IBM 360/370 host computer. IGPS allows a graphics programmer to fully explore and exploit the advanced 3-D capabilities of the Adage 4370 graphics system. It provides the user with the capability to interact with his graphics program and frees him to concentrate on the processing of data. A complete graphics system, IGPS handles consoles, does data conversion, and performs interrupt handling.

- **PORTABLE** — IGPS functions are available from COBOL, FORTRAN, and Assembly Language.

- **RE-ENTRANT** — IGPS makes extensive use of re-entrant code, ensuring minimum memory requirements for multiple graphics jobs. Any future changes in the re-entrant code for upgrading IGPS are transparent to the user.

- **FLEXIBLE** — IGPS provides the user the ability to control the data structures and parameters being handled by the package.

- **MULTI-DISPLAY** — IGPS supports any number of display stations, which can each include a variety of interactive input devices.

- **STRUCTURED** — IGPS is coded in structured modules, facilitating user additions to the package.

- **COMPLETE** — IGPS gives the user the tools to fully utilize the advanced Adage 4370 architecture.

- **MINIMUM IMPACT** — IGPS requires minimum CPU interruption through its three-level processor hierarchy (interface, control processor, and display processor).

- **VERSATILE** — Some of the many applications that can be handled by IGPS include: CAD/CAM, simulation, intelligence/signal processing, command and control, numerical control, structural analysis, and mapping and cartography.

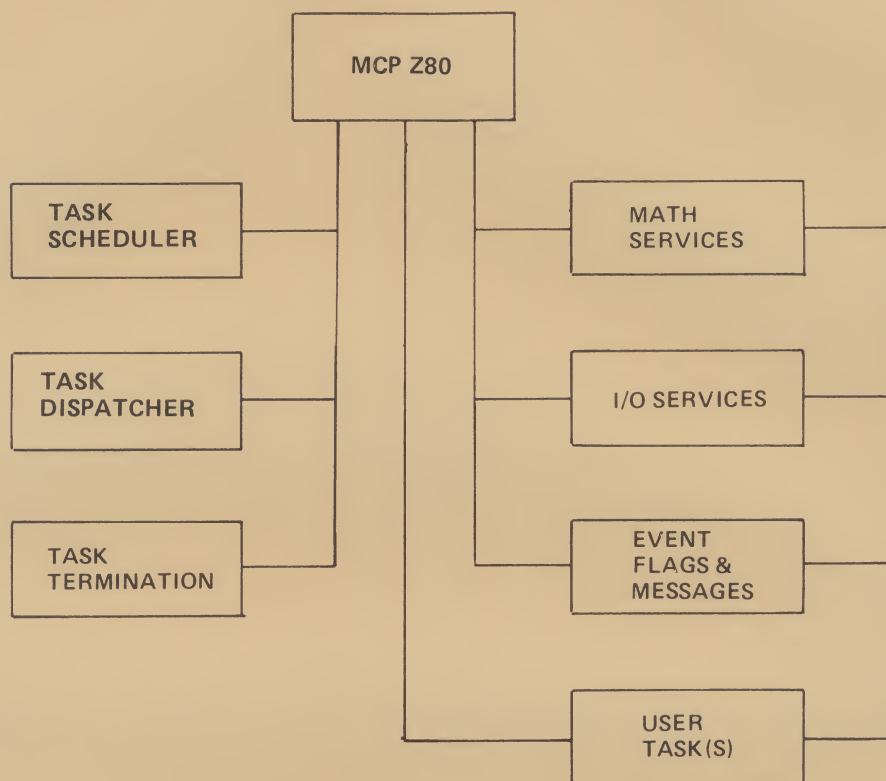


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MCP/Z80

Z-80 MULTI-TASKING EXECUTIVE



MCP/Z80 is a multitasking, real-time, priority-ordered executive for the Z-80 microprocessor.

- Priority ordered task queue
- Intertask messages
- Event flag signaling
- Dynamic RAM management
- Resident queue management
- Extensive task controls available
- PROM resident math & conversion services

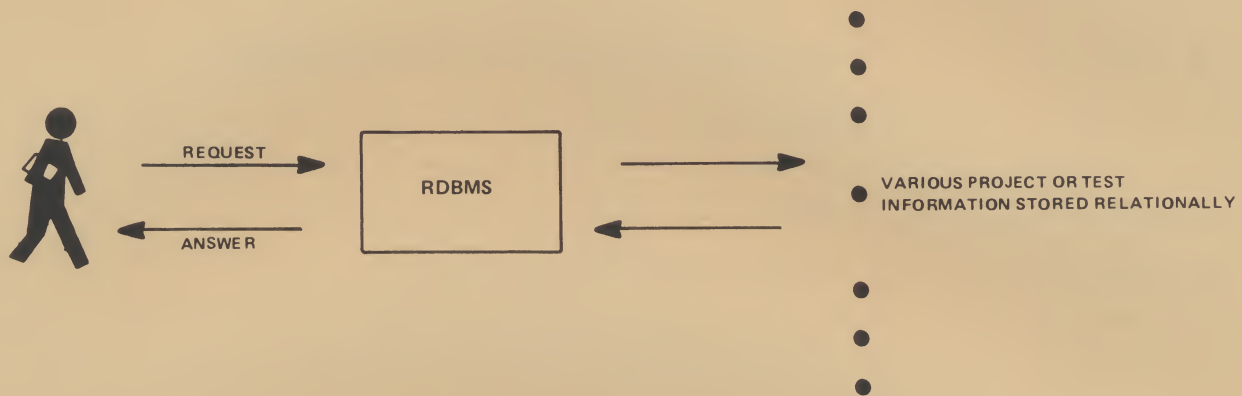


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RDBMS RELATIONAL DATA BASE MANAGEMENT SYSTEM

FOR USE IN STORING AND RETRIEVING DATA
BY USING RELATIONS OR TABLES



DATA BASE MANAGEMENT SYSTEM (DBMS)

The data processing system provides the means to access, organize, and control all information stored in the database.

The SAI RDBMS is a relational system which affords the user one simple data structure with which to view all data — the two-dimensional table called a relation. A relation contains information about an object in its rows and columns.

Advantages of RDBMS:

- SIMPLE — Two dimensional tables are easy to understand.
- FLEXIBLE — Minimal dependence of application queries upon data structure.
- POWERFUL — Operations on entire tables or relations with one command as well as row (or record) or column operations.
- PRECISE — RDBMS has a rigorous mathematical foundation as do all truly relational systems.



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RDBMS CONTINUED

RDBMS COMMANDS

- CREATE — Brings permanent relation into accessible storage.
- SELECT — Makes a new relation from existing ones.
- PROJECT — Picks off selected column information from a relation.
- JOIN — Makes a new relation from two existing ones.
- MODIFY — Replaces specific column values.
- APPEND — Adds new rows to an existing relation.
- DELETE — Removes rows from a temporary relation.
- PRINT — Prints relation.
- FOR condition — Provides qualification statements for column values for all commands above except APPEND and REPORT.

RDBMS SPECIFICATIONS

Physical characteristics of the RDBMS:

Primarily coded in ANSI 3.9 FORTRAN

Two Versions —

- 32 bit version executes on IBM 360/75
- 16 bit version executes on V77/600 which is overlayed and multi-tasked

Core Requirements:

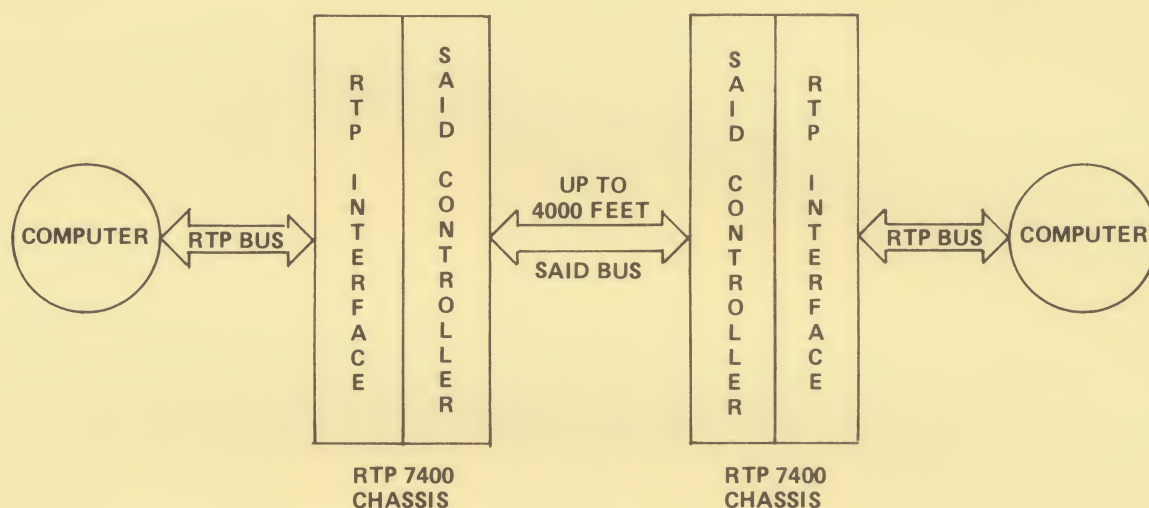
IBM Version — 236K bytes of core

V77/600 Version — Maximum 32K for a task (eight tasks)

SAITM PARALLEL INTERPROCESSOR LINK FOR USE WITH



- DEC PDP-8E
- DEC LSI-11 SERIES
- VAX 11/780
- DEC 10
- DEC PDP-11 SERIES
- SEL 32/77 SERIES
- HARRIS SLASH SERIES
- HEWLETT PACKARD 21 MX SERIES
- MODCOMP
- HONEYWELL SERIES 60 (LEVEL 6)
- ECLIPSE
- NOVA
- MICRONOVA
- PERKIN-ELMER (INTERDATA)
- INTEL SBC 80;86
- TI 990 SERIES
- MOTOROLA 6800
- SPERRY COMPUTERS (VARIAN)
- IBM SERIES/1
- GENERAL AUTOMATION



SAI — PARALLEL DIFFERENTIAL INTERPROCESSOR LINK BETWEEN ANY TWO COMPUTERS LISTED AND IN ANY COMBINATION

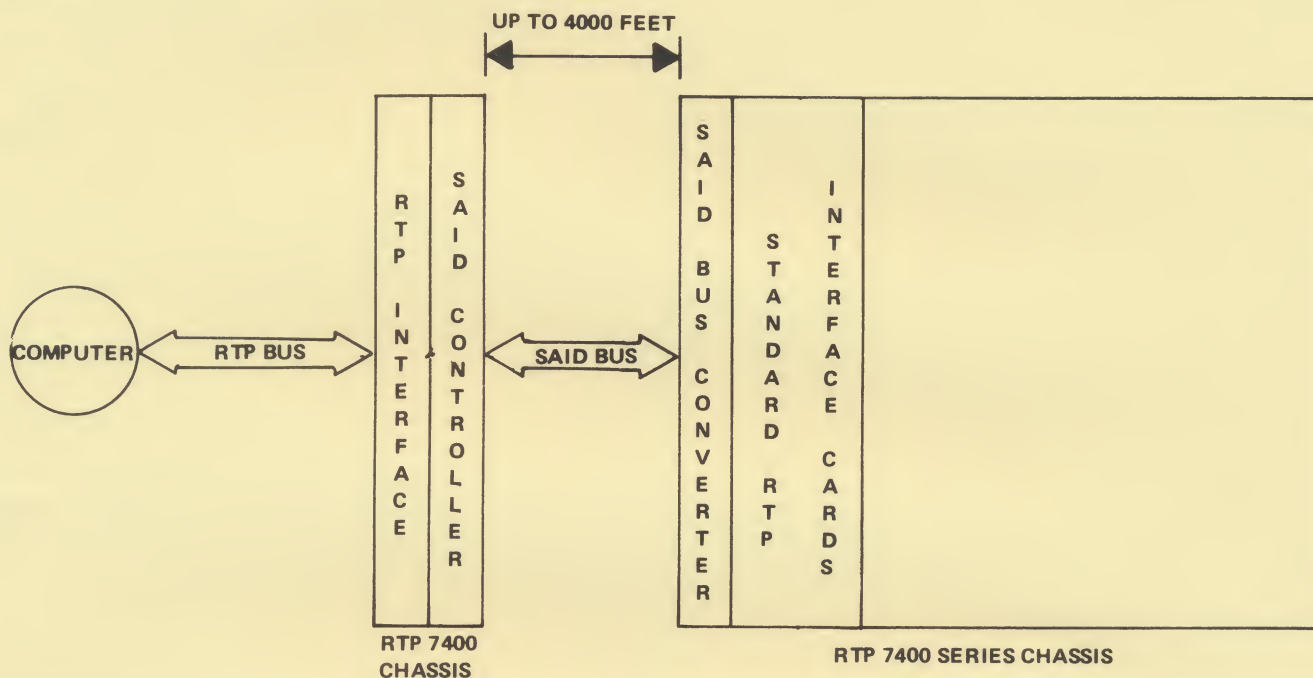
- Interfaces with Standard Computer Products RTP Bus Converters and RTP Chassis
- Differential Drivers and Receivers — EIA RS 422
- High Speed Parallel Data Transfer at Distances to 4000 Feet
- Single and Double Bit Error Detection
- 16-Bit Status Word
- Single Bit Error Correction
- Permits a Distributed System of up to 80 nodes
- Software Drivers for DEC PDP 11, LSI 11/2, LSI 11/23 and SEL 32 Series Computers
- COMING — SAITM BUS ARBITRATOR FOR MULTIPROCESSOR OPERATION ON A SINGLE SAITM BUS



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COMPUTER PRODUCTS RTP CHASSIS REMOTE LINK



Allows the location of the Computer Products RTP chassis up to 4000 feet from host computer using SAI's SAID™ Bus.

SAID™ to RTP Bus Converter provides a parallel differential link up to 4000 feet when coupled with a SAID™ controller.

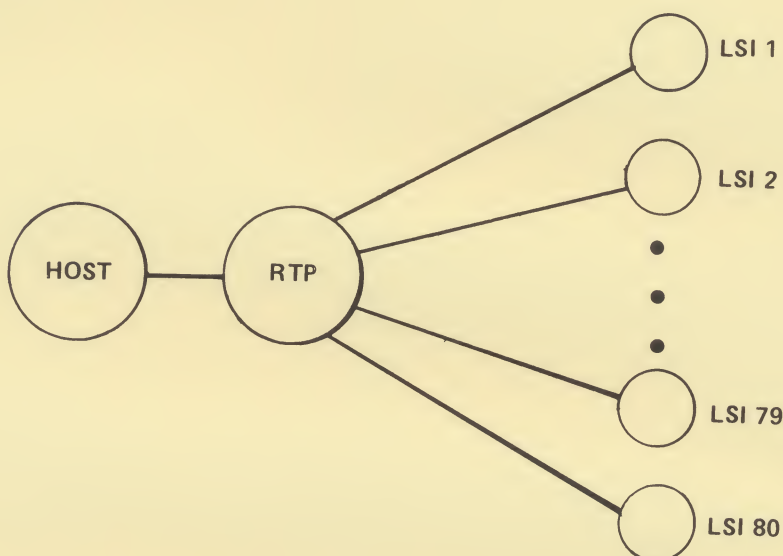
- EIA RS 422 Differential Drivers/Receivers
- Single and Double Bit Error Detection
- Single Bit Error Correction
- High Speed Parallel Data Transfer to 4000 Feet
- 16 Bit Internal Status Word
- Provides Interrupt Polling Via the SAID™ controller
- Receives Commands and Data from the SAID™ Controller

Remote RTP chassis supports full range of Computer Products I/O cards.





COMPUTER PRODUCTS RTP TO DEC LSI II INTERFACE



Parallel DMA interface between Computer Products RTP Chassis and an LSI-11 DRV11-B.

- Sequential/Random Modes
- Single Ended I/O Drivers and Receivers
- Loop Test Modes
- 16-Bit status word readable by the Host Processor
- Interfaces with standard Computer Products RTP 7430 series chassis
- Software drivers available for LSI 11/2, 11/23

OPTIONS:

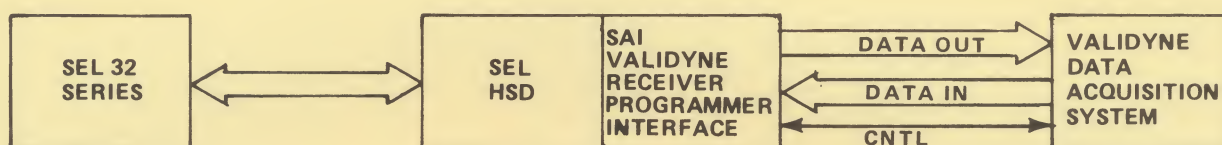
- Multiplexer system for random or sequential control of up to 10 LSI's.
- Expandable to 80 LSI's in random mode only.



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SEL 32 SERIES VALIDYNE INTERFACE



- Converts the HSD 32-bit Bidirectional Data Bus to 16-bit Unidirectional I/O Buses
- Compatible with the SEL 32 Series HSD
- Compatible with Validyne MR312 Master Receiver
- Built-in Self-Test Mode
- Compatible with the SEL HSD Diagnostic
- Fabricated on SAI's SEL Compatible Wire Wrap Board
- SAI's HSD Driver is available for MPX Version 1.4.



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GRINNEL GRAPHICS SYSTEM HIGH SPEED INTERFACE FOR SEL 32 SERIES COMPUTERS



SAI GRINNEL INTERFACE:

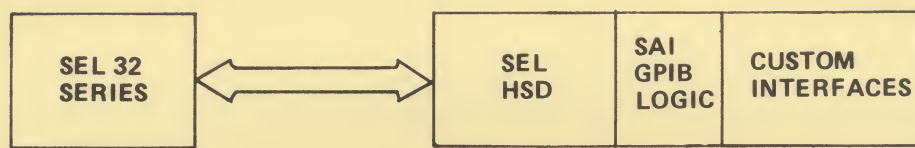
- Converts the SEL HSD 32-Bit Bidirectional Data Bus to 16-Bit Unidirectional I/O Buses
- Compatible with the SEL 32 Series HSD
- Compatible with GRINNEL Models GMR 26 or 27
- Built-in Self-Test Mode
- Compatible with the SEL HSD Diagnostic
- Fabricated on SAI's SEL Compatible Wire Wrap Board
- SAI's HSD Driver is available for MPX Version 1.4.



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SEL 32 SERIES HSD GENERAL PURPOSE INTERFACE



SAI GPIB INTERFACE:

- Contains Basic Interface Logic
- Provides User with capability of implementing custom logic
- Contains all control logic necessary to implement input and output transfers
- Compatible with the SEL 32 Series HSD
- Contains 32-bit Input/Output Data Registers
- Built-in Self-Test Mode
- Compatible with the SEL HSD Diagnostic
- Fabricated on SAI's SEL Compatible Wire Wrap Board
- SAI's General Purpose HSD Driver is available for MPX Version 1.4.





SEL 32 SERIES HSD UNIVERSAL WIRE WRAP BOARD SAI MODEL 32-9101



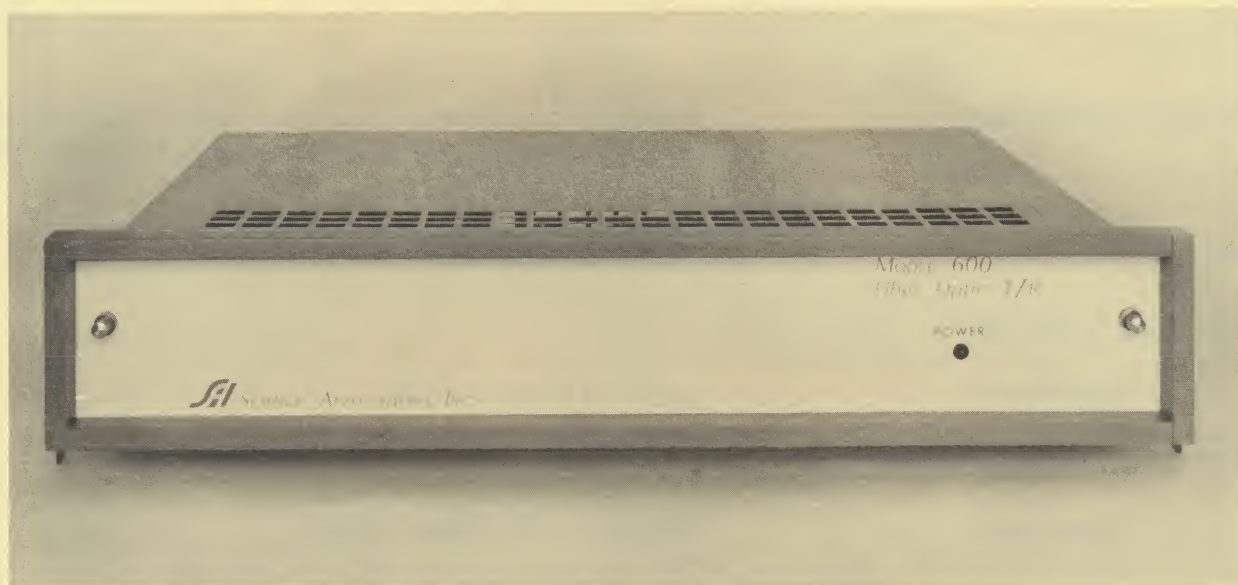
- COMPATIBLE WITH THE SEL 32 SERIES CHASSIS
- FOUR 50 PIN I/O CONNECTOR SLOTS
- BY-PASS CAPACITOR SLOTS PROVIDED
- ROWS 'A' AND 'B' ACCOMMODATE UP TO 16 PIN DIPS
- ROWS 'C' AND 'D' ACCOMMODATE UP TO 40 PIN DIPS
- ROW 'E' HAS PROVISION FOR 20 PIN DIPS
- PROVISIONS FOR UP TO 120 16 PIN DIPS
- SOCKET TERMINAL BOARD



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Huntsville, AL 35895
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FIBER OPTIC LINK SAI MODEL 600 T/R



The SAI Model 600 Fiber Optic Transmitter/Receiver (T/R) is designed to be used in pairs with two graded index optical fibers to form an electro-optical repeater subsystem which permits the location of a Computer Products RTP chassis up to 1500 meters away from the controlling SEL 32 series computer.

The SAI Model 600 Fiber Optic T/R:

- Connects between the SEL Model 7410 Analog Digital Interface (ADI) board and the first Real Time Peripheral (RTP) chassis
- Supports full data rate of the ADI-RTP subsystem
- Is functionally transparent to user
- Uses ITT Fiber Optic Transmitter/Receiver Modules and is compatible with ITT T-1200 series graded index optical fibers
- Options:
 - ▲ RS-232, RS-422, RS-423, TTL compatible input/output interfaces
 - ▲ Custom Interface Logic Cards



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MODEL 600 FIBER OPTIC T/R

SPECIFICATIONS

Electrical Input/Output: Transformer coupled TTL Type Signal (Compatible with SEL Model 130-103030-000 Serial Data Interface Receiver/Transmitter)

Maximum Frequency: 10 MHz Square Wave

Fiber Optic Transmitter

Type/Model: LED — ITT Model T-6011

Fiber Optic Receiver

Type/Model: Pin Diode — ITT Model T-6061

Physical/Environmental

Weight: 15 lbs (6.8 KG)
Height: 3.5 inches (8.9 CM)
Width: 19 inches (48.3 CM)
Depth: 12 inches (30.5 CM)
Power: 115V AC 60 Hz 1 ϕ
Fuse: 3AG 0.5 AMP SLO-BLO

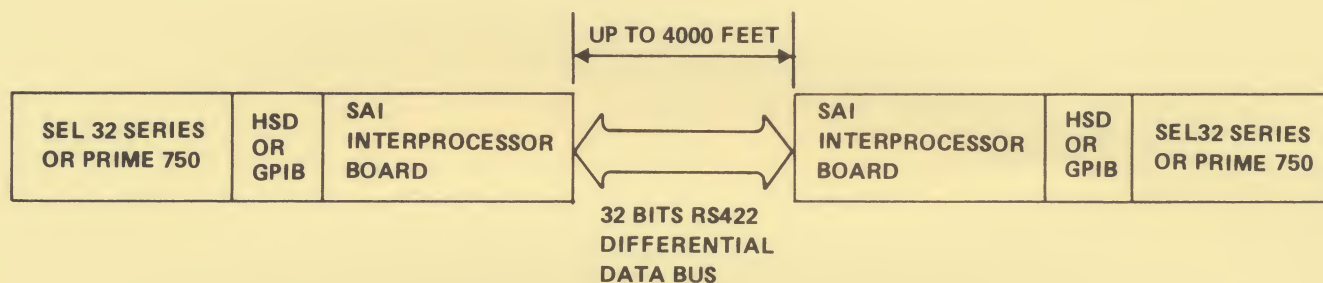
Connectors

Electrical: SMA-OSM-215SF
Optical Fiber: ITT Cannon Unilux/FOT



PARALLEL DMA INTERPROCESSOR LINK

- SEL TO PRIME
- SEL TO SEL
- PRIME TO PRIME



- Utilizes SEL HSD and/or Prime GPIB Interfaces
- EIA RS422 Differential Drivers and Receivers
- High Speed Parallel Data Transfer at Distances to 4000 Feet
- Software Drivers Available



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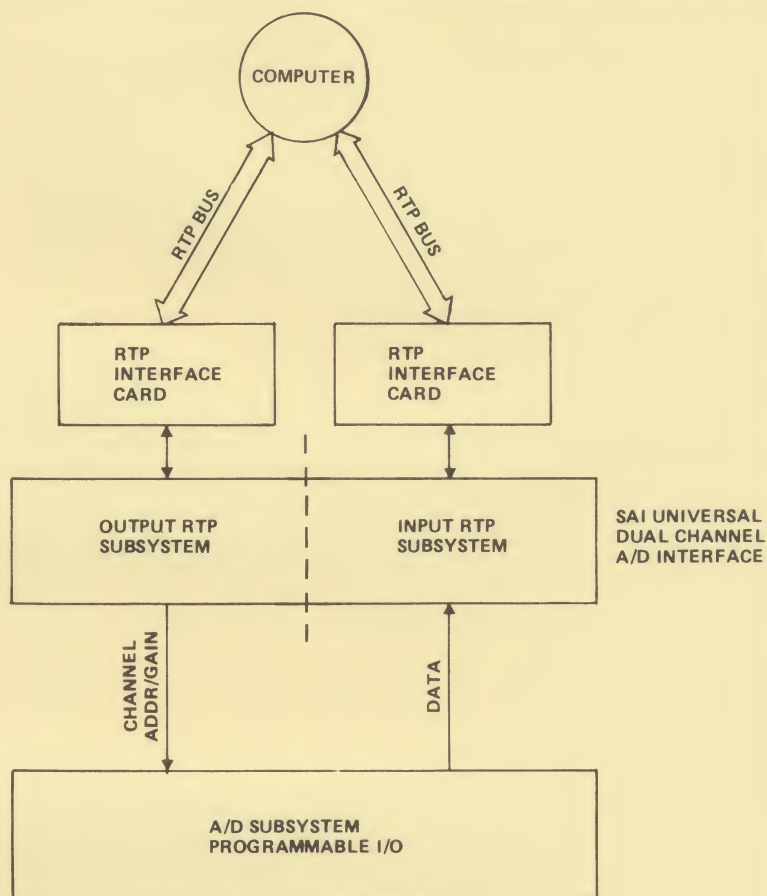


UNIVERSAL A/D INTERFACE

COMPATIBLE WITH
COMPUTER PRODUCTS RTP 7400 SERIES

SAI UNIVERSAL DUAL CHANNEL A/D
SUBSYSTEM INTERFACE FOR USE WITH:

- DEC PDP-8E
- DEC LSI-11 SERIES
- DEC 10
- DEC PDP-11 SERIES
- VAX 11/780
- SEL 32/77 SERIES
- HARRIS SLASH SERIES
- HEWLETT PACKARD 21 MX SERIES
- MODCOMP
- HONEYWELL SERIES 60 (LEVEL 6)
- ECLIPSE
- NOVA
- MICRONOVA
- INTEL SBC 80,86
- MOTOROLA 6800
- IBM SERIES/1



- PERKIN-ELMER (INTERDATA)
- TI 990 SERIES
- SPERRY COMPUTERS (VARIAN)
- GENERAL AUTOMATION

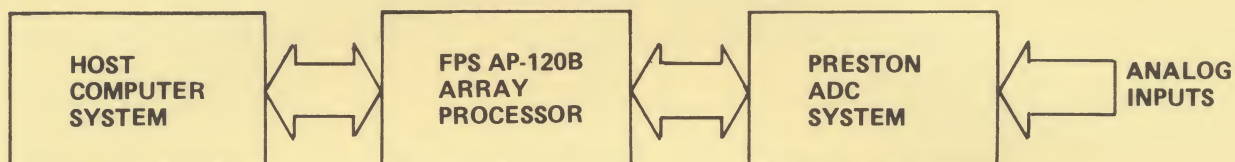
PROGRAMMABLE INPUT/OUTPUT CARDS:

- Receiver input bias for logic level conversion
- Receiver polarity selection
- Driver positive/negative true output selection
- Independent input/output channels
- Output FIFO stack for channel address and gain
- Input FIFO stack for data input





HIGH-SPEED DATA ACQUISITION AND PROCESSING SYSTEMS



FEATURES

- High-Speed Analog-to-Digital Conversion, Data Acquisition and Real-Time Processing
- Fully Integrated Turnkey Systems — Hardware and Software
- Systems Engineering, Design and Implementation Services

PRESTON GM SERIES ADC SYSTEMS

- Up to 900 kHz Conversion Rates
- 8 Bit to 15 Bit Resolution
- Programmable Conversion Rates and Gain Amplifiers
- Signal Conditioning, Amplification, Filtering, Sample-and-Hold, Multiplexing

FLOATING POINT SYSTEMS AP-120B ARRAY PROCESSOR

- DMA Data Transfers to Preston ADC and Host Computer System
- 12 Megaflops (Million Floating Point Operations Per Second) Throughput
- 38 Bit Floating Point Precision

HOST COMPUTER SYSTEM

- DEC VAX-11/780
- DEC PDP-11 Series
- HARRIS 100, 500, 800 Series
- PRIME
- SEL 32 Series

APPLICATIONS AREAS

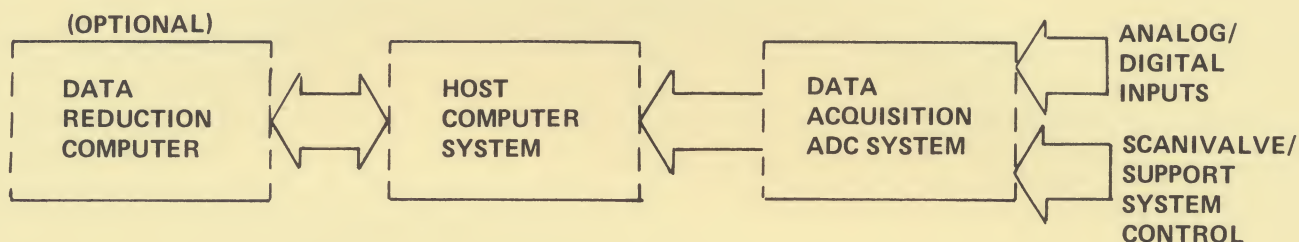
- Jet Engine and Wind Tunnel Testing
- Image and Signal Processing
- Seismic Exploration
- Vibration and Structural Analysis



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WIND TUNNEL DATA ACQUISITION SYSTEM



FEATURES

- High-Speed Analog-to-Digital Conversion, Support System (model movement) and Scanivalve Control, Data Acquisition and Real-Time Display and Processing
- Modular configuration/reconfiguration of front end, adaptable to different front-end equipment
- Fast set-up of test definitions, easy man-machine interface
- Local or remote automatic transfer and archiving of test data
- Fully integrated Turnkey Systems — Hardware and Software
- System Engineering Design, Implementation, and Training Services

FRONT END ADC SYSTEMS

- Up to 1 MHz Conversion Rates, up to 15 Bit Resolution
- Up to 50 kHz Conversion Rates, up to 16-Bit Resolution
- Programmable Gain Amplifiers
- Signal Conditioning, Amplification, Filtering, Sample-and-Hold, Multiplexing

HOST COMPUTER SYSTEMS

- DEC VAX-11/780 or 11/750, PDP-11 Series
- SEL 32 Series, PRIME, HARRIS, PERKIN-ELMER Re-hosting available

APPLICATIONS AREAS

- Wind Tunnel, Inlet and Duct Testing
- Balance/Transducer Calibration Laboratory



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